

CLAIMS:

1. A semiconductor memory device comprising;  
a memory portion which allows data to be re-  
written,

an internal circuit having a plurality of  
operation modes designated by the function signal  
and deciding data to be offered to said memory por-  
tion in each operation mode,

an address input terminal, and

a function setting circuit in which the input  
signal to be taken thereinto is fed via said address  
input terminal to form said function signal in ac-  
cordance with said input signal.

2. A semiconductor memory device as defined in  
Claim 1, wherein said device comprises a timing con-  
trol circuit which receives a substantial chip se-  
lection signal and a first control signal and when  
said chip selection signal and said control signal  
are altered by the predetermined combination, forms  
a first timing signal, said function setting circuit  
taking in the input signal in accordance with said  
first timing signal.

3. A semiconductor memory device as defined in  
Claim 2, wherein said function setting circuit has a  
hold means for maintaining the level of said function

4 signal until said first timing signal is again  
5 generated.

1 4. A semiconductor memory device as defined in  
2 Claim 2, wherein it comprises an address buffer the  
3 input terminal of which is coupled to said address  
4 input terminal, the input signal being fed via said  
5 address buffer to said function setting circuit.

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1 5. A semiconductor memory device as defined in  
2 Claim 4, wherein said address buffer comprises an  
3 address buffer for receiving the row address signal  
4 and the column address signal which are fed to said  
5 address input terminal in accordance with the time  
6 sharing system and said chip selection signal com-  
7 prises the row address strobe signal, and said first  
8 control signal is composed of the column address  
9 strobe signal and the write enable signal.

1 6. A semiconductor memory device as defined in  
2 Claim 5, wherein said memory portion comprises a  
3 dynamic random access memory.

1 7. A semiconductor memory device as defined in  
2 Claim 6, wherein it comprises further a refresh con-  
3 trol circuit for forming at least the refresh address  
4 strobe signal for said memory portion and said timing  
5 control circuit makes the refresh operation effective  
6 by said refreshing control circuit in response to the

6/ 7 column address strobe signal being set to the active  
8 level when said row address strobe signal is set  
9 to the inactive level and the timing signal is formed  
10 so that the input operation of said function setting  
11 circuit may be made effective in response to the  
12 status wherein, said row address strobe signal and  
13 the column address strobe signal are respectively  
14 set to the inactive and active levels, while the  
15 write enable signal is set too the active level.

1 8. A semiconductor memory device as defined in  
2 Claim 7, wherein said internal circuit comprises an  
3 operation circuit whose operation mode is designated  
4 by the function signal fed from said function setting  
5 circuit, while forming data to be offered to said  
6 memory portion in accordance with the input data and  
7 the data to be read out from said memory portion.

1 9. A semiconductor memory device comprising;  
2 a memory portion which allows data to be re-  
3 written,

4 an operation circuit for forming the operation  
5 data to be written in said memory portion, receiving  
6 the input data and the data to be read out from said  
7 memory portion,

8 a function circuit, and

9 a bypass circuit the operation of which is

10 controlled by the control signal fed from said func-  
11 tion setting circuit and which, in the operated  
12 state, feeds said input data directly to said memory  
13 portion.

a) 1 10. A semiconductor memory device as defined in  
2 Claim 9, wherein said operation circuit has a plu-  
3 rality of operation modes and said function setting  
4 circuit outputs the operation control signal for  
5 controlling said operation mode.

1 11. A semiconductor memory device as defined in  
2 Claim 10, wherein it comprises further a timing con-  
3 trol circuit the operation of which is controlled  
4 by a plurality of external control signals and when  
5 said plurality of external control signals are set  
6 to the predetermined state, form the control signal  
7 for setting said function setting circuit to the  
8 state of input operation, said function setting cir-  
9 cuit having a hold means for maintaining said opera-  
10 tion control signal and said control signal for said  
11 bypass circuit after said state of input operation.

1 12. A semiconductor memory device as defined in  
2 Claim 11, wherein it has further an address input  
3 terminal and a coupling means for coupling said  
4 address input terminal and the input terminal of  
5 said function setting circuit.

a1 1 13. A semiconductor memory device as defined in  
2 Claim 12, wherein said coupling means comprises a  
3 column address buffer.

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A3 7

Add  
B1 7

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C2 7